

Question No : 1 of 26

Marks: 1 (Budgeted Time 1 Min)

The first Least Significant digit in decimal number system has

Answer (Please select your correct option)

☐ position 0 and weight equal to 1

correct

☐ position 1 and weight equal to 0

☐ position 1 and weight equal to 10

☐ position 0 and weight equal to 10

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Question No : 2 of 26

Marks: 1 (Budgeted Time 1 Min)

Consider the binary number "100101", its 2's complement will be _____

Answer (Please select your correct option)

☐ 100110

☐ 011011

correct

☐ 100111

☐ 011010

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Question No : 3 of 26

Marks: 1 (Budgeted Time 1 Min)

$$A + \overline{A}B = \underline{\hspace{2cm}}$$

Answer (Please select your correct option)

☐ A

☐ B

☐ AB

☐ $A+B$

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Question No : 4 of 26

Marks: 1 (Budgeted Time 1 Min)

According to Demorgan's theorem:

$$\overline{A + B + C} = \underline{\hspace{2cm}}$$

Answer (Please select your correct option)

☐ A.B.C

☐ $A + \overline{B.C}$

☐ $\overline{A} \overline{B} \overline{C}$

correct

☐ $\overline{A} \overline{B} + C$

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Question No : 5 of 26

Marks: 1 (Budgeted Time 1 Min)

The Extended ASCII Code (American Standard Code for Information Interchange) represents _____ unique codes

Answer (Please select your correct option)

☐ 256

correct

☐ 255

☐ 128

☐ 127

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Question No : 6 of 26

Marks: 1 (Budgeted Time 1 Min)

The three fundamental gates are _____

Answer (Please select your correct option)

☐ AND, NAND, XOR

☐ OR, AND, NAND

☐ NOT, NOR, XOR

☐ NOT, OR, AND

correct

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Question No : 7 of 26

Marks: 1 (Budgeted Time 1 Min)

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

Answer (Please select your correct option)

☐ 0

☒ 1

correct

☐ X (don't care condition)

☐ Any of given option depending on SOP term.

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Question No : 8 of 26

Marks: 1 (Budgeted Time 1 Min)

The output $A < B$ is set to 1 when the input combinations is _____

Answer (Please select your correct option)

☐ A=10, B=01

☐ A=11, B=01

☐ A=01, B=01

☐ A=01, B=10

correct

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Question No : 9 of 26

Marks: 1 (Budgeted Time 1 Min)

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

Answer (Please select your correct option)

- ☐ Using a single comparator
- ☐ Using Iterative Circuit based Comparators
- ☐ Connecting comparators in vertical hierarchy
- ☐ Extra logic gates are always required.

correct

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Question No : 10 of 26

Marks: 1 (Budgeted Time 1 Min)

Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ____ multiplexer.

Answer (Please select your correct option)

☐ 2-input, 8-bit

correct

☐ 2-input, 4-bit

☐ 4-input, 8-bit

☐ 4-input, 16-bit

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Question No : 11 of 26

Marks: 1 (Budgeted Time 1 Min)

$A.(B.C) = (A.B).C$ is an expression of _____

Answer (Please select your correct option)

☐ Demorgan's Law

☐ Distributive Law

☐ Commutative Law

☐ Associative Law

correct

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Question No : 12 of 26

Marks: 1 (Budgeted Time 1 Min)

$(A + B)(A + \bar{B} + C)(\bar{A} + C)$ is an example of _____

Answer (Please select your correct option)

☐

Product of sum form

correct

☐

Sum of product form

☐

Demorgans law

☐

Associative law

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Question No : 13 of 26

Marks: 1 (Budgeted Time 1 Min)

The expression $F=A+B+C$ describes the operation of 3-bit _____ gate.

Answer (Please select your correct option)

☐ OR

correct

☐ AND

☐ NOT

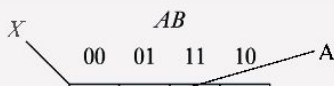
☐ NAND

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Question No : 14 of 26

Marks: 1 (Budgeted Time 1 Min)

In the following Karnaugh map, which group has "legal grouping" ?



Answer (Please select your correct option)

☐ A

☐ B

☐ C

correct

☐ D

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Question No : 15 of 26

Marks: 1 (Budgeted Time 1 Min)

A particular Full Adder has _____ inputs and _____ output(s).

Answer (Please select your correct option)

☐ 2, 3

☐ 2, 2

☐ 3, 2

correct

☐ 3, 3

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Question No : 14 of 26

Marks: 1 (Budgeted Time 1 Min)

00	1	1	1	0	
01	1	0	0	1	
11	0	1	1	1	

CD

B

C

Answer (Please select your correct option)

☐ A

☐ B

☐ C

correct

☐ D

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Question No : 14 of 26

Marks: 1 (Budgeted Time 1 Min)

<i>CD</i>					
11	0	1	1	1	
10	0	1	1	0	

Answer (Please select your correct option)

- ☐ A
- ☐ B
- ☐ C correct
- ☐ D

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Question No : 16 of 26

Marks: 1 (Budgeted Time 1 Min)

Which of the following is a symbol of OR operation in ABEL?

Answer (Please select your correct option)

☐ #

correct

☐ \$

☐ !

☐ &

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Question No : 17 of 26

Marks: 1 (Budgeted Time 1 Min)

A latch has ____ stable state(s).

Answer (Please select your correct option)

☐ One

☒ Two

☐ Three

☐ Four

correct

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Question No : 18 of 26

Marks: 1 (Budgeted Time 1 Min)

A latch retains its state unless _____

Answer (Please select your correct option)

- ☐ Power is turned off
- ☒ Input is changed
- ☐ Output is changed
- ☐ Clock pulse is changed

correct

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Question No : 19 of 26

Marks: 1 (Budgeted Time 1 Min)

At $S = 0$ and $R = 1$, an active-HIGH SR latch is in _____ condition.

Answer (Please select your correct option)

☐ SET

☐ RESET

☐ Invalid

☐ No change

correct

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Question No : 20 of 26

Marks: 1 (Budgeted Time 1 Min)

What are the sum (Σ) and the carry (C_{out}) for full adder circuit when $A = 1$, $B = 1$ and $C_{in} = 0$?

Answer (Please select your correct option)

☐ $\Sigma = 0, C_{out} = 1$

correct

☐ $\Sigma = 1, C_{out} = 0$

☐ $\Sigma = 1, C_{out} = 1$

☐ $\Sigma = 0, C_{out} = 0$

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Question No : 21 of 26

Marks: 2 (Budgeted Time 4 Min)

How many possible outputs does a decoder of 3 inputs contain?

Answer (Please [click here](#) to Add Answer)

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Decoder, the 3-to-8 Decoder has active-low outputs and three extra NOT gates connected at the three inputs to reduce the four unit load to a single unit load. The 3-to-8 Decoder has three enable inputs, one of the three enable inputs is active-high and the remaining two are active-low. All three enable inputs have to be activated for the Decoder to work

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Question No : 22 of 26

Marks: 2 (Budgeted Time 4 Min)

Once the Logic circuit design has been entered its operation is verified by using 'test vectors'. Write two major roles of test vectors.

Answer (Please [click here](#) to Add Answer)

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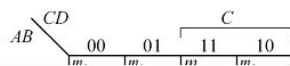
The testing verifies the design of the logic circuit before committing it to the PLD. If any flaws are detected during the testing process the design must be debugged and submitted for recompilation. Once the design has been finalized a documentation file is produced along with a fuse map file which is downloaded to the programmer which programs the PLD device inserted in the programmer socket.

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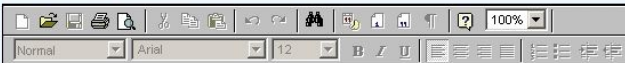
Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

Derive simplified Boolean equation from the following Karnuagh Map.



Answer (Please [click here](#) to Add Answer)



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Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

AB	C			
	00	01	11	10
00	m_0	m_1	m_3 1	m_2
01	m_4	m_5	m_7 1	m_6

Answer (Please [click here](#) to Add Answer)



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Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

$$A \begin{bmatrix} 11 \\ 10 \end{bmatrix} \begin{bmatrix} m_{12} & m_{13} & m_{15} & m_{14} \\ m_8 & m_9 & m_{11} & m_{10} \end{bmatrix} B$$

Answer (Please [click here](#) to Add Answer)

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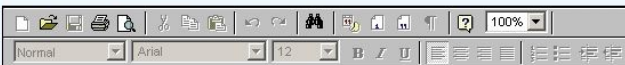
Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

$$A \begin{bmatrix} m_8 & m_9 & m_{11} & m_{10} \\ 10 & & 1 & \end{bmatrix}$$

$\underbrace{\hspace{10em}}_D$

Answer (Please [click here](#) to Add Answer)



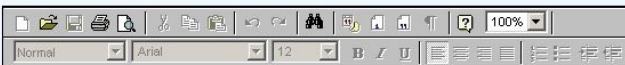
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Question No : 24 of 26

Marks: 3 (Budgeted Time 6 Min)

Tri-state buffer control input can be connected in four different ways. Name any three of them.

Answer ([Please click here to Add Answer](#))



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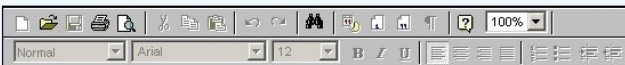
Question No : 25 of 26

Marks: 5 (Budgeted Time 10 Min)

Using Karnaugh map minimize the following POS expression:

$$(B + C + D)(A + B + \bar{C} + D)(\bar{A} + B + C + \bar{D})(A + \bar{B} + C + D)(\bar{A} + \bar{B} + C + D)$$

Answer ([Please click here to Add Answer](#))



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Question No : 26 of 26

Marks: 5 (Budgeted Time 10 Min)

Draw the function table of 8-to-3 Encoder.

Answer ([Please click here to Add Answer](#))

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