

Question No : 1 of 26

Marks: 1 (Budgeted Time 1 Min)

Consider the binary number "100101", its 2's complement will be _____

Answer (Please select your correct option)

☐ 100110

☐ 011011

correct

☐ 100111

☐ 011010

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Question No : 2 of 26

Marks: 1 (Budgeted Time 1 Min)

The values that exceed the specified range can not be correctly represented and are considered as _____

Answer (Please select your correct option)

☐ Overflow

correct

☐ Carry

☐ Parity

☐ Sign value

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Question No : 3 of 26

Marks: 1 (Budgeted Time 1 Min)

According to Demorgan's theorem:

$$\overline{A + B + C} = \underline{\hspace{2cm}}$$

Answer (Please select your correct option)

☐ $A.B.C$

☐ $A + \overline{B.C}$

☐ $\overline{A.B.C}$

correct

☐ $\overline{A.B} + C$

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Question No : 4 of 26

Marks: 1 (Budgeted Time 1 Min)

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result

Answer (Please select your correct option)

☐ 1001

☐ 0110

☐ 1111

☐ 1100

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Question No : 5 of 26

Marks: 1 (Budgeted Time 1 Min)

The output of an AND gate is one when _____

Answer (Please select your correct option)

☐ All of the inputs are one

correct

☐ Any of the input is one

☐ Any of the input is zero

☐ All the inputs are zero

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Question No : 6 of 26

Marks: 1 (Budgeted Time 1 Min)

A standard SOP form has _____ terms that have all the variables in the domain of the expression.

Answer (Please select your correct option)

☐ Sum

☐ Product

correct

☐ Max

☐ Composite

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Question No : 7 of 26

Marks: 1 (Budgeted Time 1 Min)

A comparator circuit has multiple inputs and _____ outputs

Answer (Please select your correct option)

☐ 2

☐ 3

correct

☐ 4

☐ 7

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Question No : 8 of 26

Marks: 1 (Budgeted Time 1 Min)

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

Answer (Please select your correct option)

- ☐ Using a single comparator
- ☐ Using Iterative Circuit based Comparators
- ☐ Connecting comparators in vertical hierarchy
- ☐ Extra logic gates are always required.

correct

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Question No : 9 of 26

Marks: 1 (Budgeted Time 1 Min)

The active high and active low inputs of 3-to-8 Decoder are as follows:

Answer (Please select your correct option)

☐ One active-high and the remaining two are active-low.

correct

☐ Two active-high and the remaining one is active-low.

☐ All active high

☐ All active low

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Question No : 10 of 26

Marks: 1 (Budgeted Time 1 Min)

OLMC consists of a _____

Answer (Please select your correct option)

☐ Encoder

☐ Decoder

☐ Logic Gate

☐ Flip-Flop

correct

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Question No : 11 of 26

Marks: 1 (Budgeted Time 1 Min)

The Quad Multiplexer has ____ inputs

Answer (Please select your correct option)

☐ 4

☐ 8

☐ 12

☐ 16

correct

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Question No : 12 of 26

Marks: 1 (Budgeted Time 1 Min)

The carry propagation can be expressed as _____.

Answer (Please select your correct option)

☐ $C_p = AB$

☐ $C_p = A + B$

☐ $C_p = A \oplus B$

☐ $C_p = A + \bar{B}$

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Question No : 13 of 26

Marks: 1 (Budgeted Time 1 Min)

In the binary number "1100.111", the first bit at the right of decimal point has the weight

Answer (Please select your correct option)

☐ $\frac{1}{2}$ (1 divided by 2)

☐ $\frac{1}{4}$ (1 divided by 4)

☐ 0

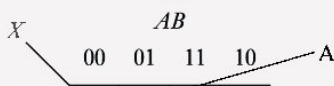
☐ 1

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Question No : 14 of 26

Marks: 1 (Budgeted Time 1 Min)

In the following Karnaugh map, which group has "legal grouping" ?



Answer (Please select your correct option)

☐ A

☐ B

☐ C

correct

☐ D

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Question No : 15 of 26

Marks: 1 (Budgeted Time 1 Min)

In CMOS 5 Volt series, Input voltage for Logic high signal (V_{IH}) is in the range of _____ volts.

Answer (Please select your correct option)

☐ 3.5 to 5

correct

☐ 4.5 to 5

☐ 0 to 5

☐ 0 to 3.5

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Question No : 16 of 26

Marks: 1 (Budgeted Time 1 Min)

Programmable Array Logic (PAL) has _____ input(s) and _____ output(s).

Answer (Please select your correct option)

☐ Single, multiple

☐ Multiple, single

☐ Single, single

☐ Multiple, multiple

correct

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Question No : 17 of 26

Marks: 1 (Budgeted Time 1 Min)

An equivalent ABEL notation of Boolean expression $A+B$ is _____

Answer (Please select your correct option)

☐ A & B

☐ A ! B

☐ A # B

correct

☐ A \$ B

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Question No : 18 of 26

Marks: 1 (Budgeted Time 1 Min)

Which circuit has the following Sum and CarryOut expressions?

$$\text{Sum} = A \oplus B \oplus C$$

$$\text{CarryOut} = C(A \oplus B) + AB$$

Answer (Please select your correct option)

☐ Half Adder

☐ Full Adder

correct

☐ 3-bit parallel adder

☐ MSI adder circuit

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Question No : 19 of 26

Marks: 1 (Budgeted Time 1 Min)

From the truth table below, determine the standard SOP expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0

Answer (Please select your correct option)

☐ $\bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C}$

☐ $AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC$

correct

☐ $(A + B + \bar{C})(A + \bar{B} + \bar{C})(\bar{A} + \bar{B} + C)$

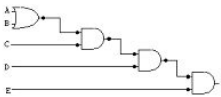
☐ $(\bar{A} + \bar{B} + C)(\bar{A} + B + C) + (A + B + \bar{C})$

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Question No : 20 of 26

Marks: 1 (Budgeted Time 1 Min)

The Boolean expression for the logic circuit is _____



Answer (Please select your correct option)

☐ AB+CDE

☐ (A+B)CDE

correct

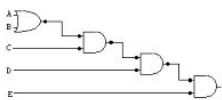
☐ (A+B)+(CDE)

☐ (A+B)(CD+E)

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Question No : 20 of 26

Marks: 1 (Budgeted Time 1 Min)



Answer (Please select your correct option)

☐ $AB+CDE$

☐ $(A+B)CDE$

correct

☐ $(A+B)+(CDE)$

☐ $(A+B)(CD+E)$

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Marks: 2 (Budgeted Time 4 Min)

Answer (Please [click here](#) to Add Answer)

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Question No : 22 of 26

Marks: 2 (Budgeted Time 4 Min)

Write down four uses of multiplexers.

Answer ([Please click here to Add Answer](#))

Normal Arial 12 B I U

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Question No : 23 of 26

Marks: 3 (Budgeted Time 6 Min)

For a two bit comparator circuit, specify all the inputs for which the output $A = B$ is set to 1.

Answer ([Please click here to Add Answer](#))

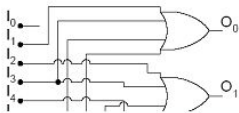


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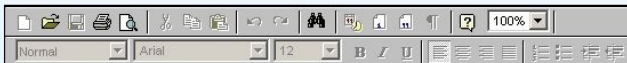
Question No : 24 of 26

Marks: 3 (Budgeted Time 6 Min)

Identify the following circuit that is which combinational circuit is being represented by this diagram?



Answer ([Please click here to Add Answer](#))



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Question No : 25 of 26

Marks: 5 (Budgeted Time 10 Min)

Map the following POS expression on a karnaugh map:

$$(\bar{A} + \bar{B} + C + D)(\bar{A} + B + \bar{C} + \bar{D})(A + B + \bar{C} + D)(\bar{A} + \bar{B} + \bar{C} + \bar{D})(A + B + \bar{C} + \bar{D})$$

Answer ([Please click here to Add Answer](#))

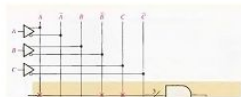


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Question No : 26 of 26

Marks: 5 (Budgeted Time 10 Min)

A programmed array is shown in Figure below. The intact fusible link, are indicated by small red Xs. Absence of an X means that the fuse is open. Analyze the figure below and write the output expression.



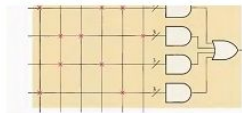
Answer ([Please click here to Add Answer](#))

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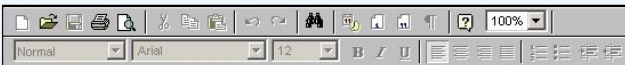
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Question No : 26 of 26

Marks: 5 (Budgeted Time 10 Min)



Answer ([Please click here to Add Answer](#))



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